AMPAK

AP6212

Evaluation Kits

User manual

Version 1.0

Revision History

Date	Revision Content	Revised By	Version
2015/1/27	Initial released	Eason	1.0

1. AP6212 Evaluation Board Introduction

AP6212 Evaluation board (EVB) likes as figure1. That is designed for IEEE802.11 /b/g/n/ WLAN with integrated Bluetooth application. It is subject to provide a convenient environment for customer's verification on WiFi or Bluetooth function. There are many controller pins and reserved GPIO on Evaluation board which describes as below.

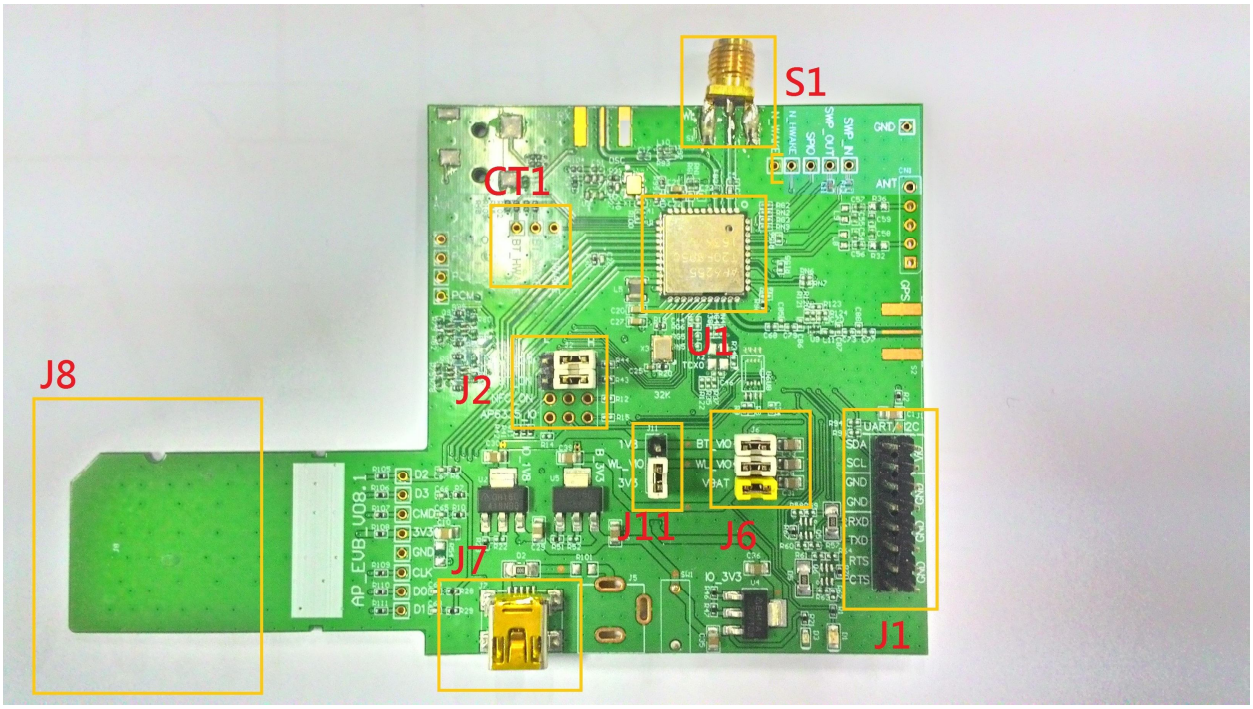

Figure1. Top view of AP6212 EVB

Interface highlights:

1. U1: AP6212 SIP module.
2. J1: UART interface connects with UART transport board for BT measuring
3. J2: Enable(H) or disable(L) Bluetooth, WiFi, and AP6335_SDIO I/O voltage selection.(H for SDIO 3.3V, L for SDIO 1.8V)
4. J6: VBAT / WL_VIO / BT_VIO for main system I/O power path.
5. J7: 5V DC mini USB input connector.
6. J8: Standard SDIO interfaces for Wi-Fi performance measured.
7. J11: WL_VIO power path for 1V8 or 3V3 selection.
8. S1: SMA connector let RF signal in/out path, you could connect with RF cable or Dipole antenna.
9. Ct1: WLAN and BT control pins, strongly recommended WL_HWAKE(IRQ) connected to MCU.

2. WiFi function verification step

WIFI SDIO: Using external pull up resistors depends on the SDIO supply voltage. For 1.8V, the resistance range is 30KΩ~82KΩ. For 3.3V, its range from 21 KΩ~41 KΩ on the four data lines and the CMD line as the following circuitry.

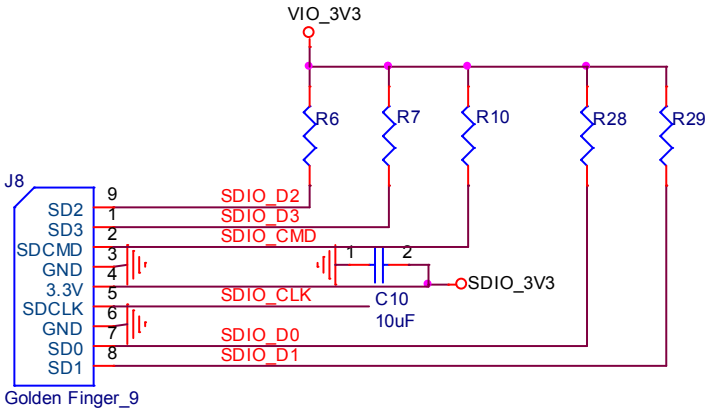

Figure2. WiFi verification connection interface to Host SDIO

Hardware Setup:

- Refer to Figure2 SDIO pin definition connects the J8 interface of AP6XXX evaluation board to Host SDIO control interface.
- Using pull high resistors (R6, R7, R10, R28, R29) that resistance is 30Kohm for 1.8V or 3.3V VDDIO pull up voltage. (Pull high resistors are un-necessary if at verification phase.)
- Connects an external antenna at SMA connector on the evaluation board.
- Note to the VDDIO voltage level should be the same with GPIO voltage level of Host CPU. (VDDIO 3.3V or 1.8V selection by jump J11)

WiFi software setup:

Please follow up software guideline of Ampak official released.

3. Bluetooth function verification step

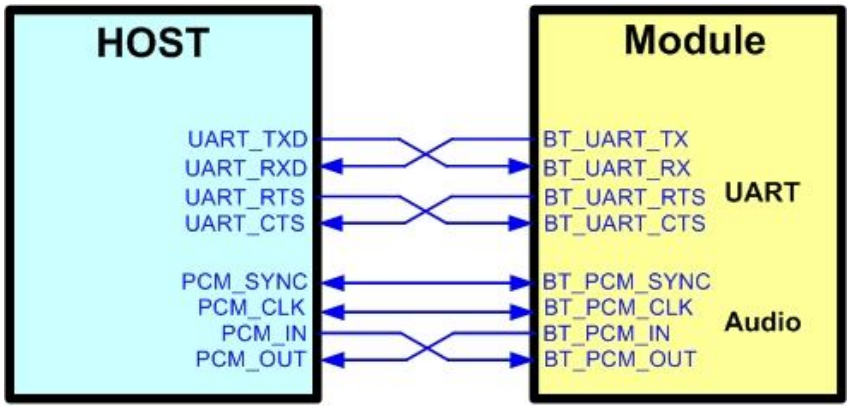

Figure3. Bluetooth verification connection interface to Host UART

Hardware Setup:

- ❖ Refer to Figure3 UART pin definition connects the J1 interface of AP6212 evaluation board to Host UART control interface.
- ❖ Connects an external antenna at SMA connector on the evaluation board.
- ❖ Note to the VDDIO voltage level should be the same as GPIO voltage level of Host CPU.

WiFi and Bluetooth software setup:

Please follow up software guideline of Ampak official released.